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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/235,770	01/25/1999	SHUNPEI YAMAZAKI	0756-1914	4196

7590

06/04/2002

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EXAMINER

SCHILLINGER, LAURA M

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 06/04/2002

21

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/235,770

Applicant(s)

YAMAZAKI ET AL.

Examiner

Laura M Schillinger

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

Applicant provided certified translations of foreign priority documents : 4-124324 and 4-113027, however has failed to include a foreign translation of JP 4-102202 priority therefore cannot be established to overcome Wakai reference and the following rejections based thereon.

Oath/Declaration

Furthermore, Applicant's declaration must have a parent application identified in order to obtain the earlier priority date.

Art Unit: 2813

Priority

2. Applicant's translation of foreign priority documents fails to contain any information pertaining to hydrogen doping nor a hydrogen containing layer- priority documents fail to support claims 2, 5, 7, 8, 9, 11, 12-14.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-5, 7-8, 10-12, 14-15, 17-18, and 20-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Wakai ('230).

In reference to claim 1, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9

(6));

another SiO layer and SiN layer on top of the semiconductor layer, (Fig.9 (7) and Col.4, lines: 1-10) and a gate (Fig.9 (8)).

Art Unit: 2813

In reference to claim 2, Wakai teaches wherein the top SiN layer is doped with H and O (Col.4, lines: 10-20).

In reference to claim 4, Wakai teaches a device comprising:

- a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

- a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

- a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig 9 (6));

- another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

- a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

- and a gate electrode formed over a channel (Fig.9 (8)).

In reference to claim 5, Wakai teaches wherein the second SiN film is doped with H and O (Col.4, lines:10-20) .

In reference to claim 7, Wakai teaches a device comprising:

- a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

- a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

Art Unit: 2813

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig 9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

and a gate electrode formed over a channel (Fig.9 (8));

wherein the source and drain regions are doped with H (Col.4, lines: 10-25).

In reference to claim 8, Wakai teaches wherein the SiN layer is doped with H or O (Col.4, lines: 10-25).

In reference to claim 10, Wakai teaches a device comprising:

a substrate (Fig.9 (1));

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig 9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

Art Unit: 2813

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

and a gate electrode formed over a channel (Fig.9 (8)).

In reference to claim 11, Wakai teaches wherein the second SiN film is doped with H or O (Col.4, lines: 10-25).

In reference to claim 12, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9 (6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

wherein the source and drain regions are doped with H (Col.4, lines: 10-25).

In reference to claim 14, Wakai teaches wherein the gate electrode is adjacent to the channel (Fig.9 (8)).

Art Unit: 2813

In reference to claim 15, Wakai teaches a device comprising:

- a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

- a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

- a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9 (6));

- another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

- a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);

- wherein both SiN layers are formed between the N and P TFTs (Fig.9 (7) and Col.4, lines: 1-10).

In reference to claim 17, Wakai teaches further comprising a gate electrode adjacent to the channel (Fig.9 (8)).

In reference to claim 18, Wakai teaches a device comprising:

- a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

- a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

Art Unit: 2813

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9

(6);

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9
(7) and Col.4, lines: 1-10);

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9
(7) and Col.4, lines: 1-10);

a gate electrode formed over the channel region (Fig.9 (8));

at least one electrode formed on the interlayer insulating film wherein at least one
electrode is connected to one of the source and drain regions via a contact hole through the
interlayer insulating film and upper two insulating films (Fig.9 (11)).

In reference to claim 20, Wakai teaches a device comprising:

a first layer of SiN formed on a substrate (Fig 9 (1a) and Col.5, lines:1-5);

a layer of SiO formed on the SiN layer (Fig 9 (1a) and Col.5, lines:1-5);

a semiconductor layer formed on the SiO layer, having a source, drain and channel (Fig.9
(6));

another SiO layer which extends the beyond the edges of the semiconductor layer (Fig.9
(7) and Col.4, lines: 1-10);;

Art Unit: 2813

a second SiN layer which extends the beyond the edges of the semiconductor layer (Fig.9 (7) and Col.4, lines: 1-10);;

a gate electrode formed over the channel region (Fig. 9 (8));

at least one electrode formed on the interlayer insulating film wherein at least one electrode is connected to one of the source and drain regions via a contact hole through the interlayer insulating film and upper two insulating films (Fig.9 (11)).

In reference to claim 21, Wakai teaches wherein the semiconductor is crystalline Si (Col.3, lines: 45-50).

In reference to claim 22, Wakai teaches wherein the substrate is glass (Col.2, lines: 60-65).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2813

6. Claims 3, 6, 9, 13, 16, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakai ('230).

In reference to claims 3, 6, 9, 13, 16, 19 applicant claims wherein the first SiN layer is 10-50 nm and the first SiO layer is 10-800 nm, and the second SiO layer is 50-200 nm, and the second SiN layer is 2-20 nm. Wakai teaches all of the above device components however fails to explicitly teach their thicknesses.

However, these claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-F 7:00 -4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1500.

LMS
May 31, 2002


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